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Design of a Low Drop-Out Voltage Regulator using VLSI

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Abstract: A Low-Voltage Low-Dropout(LDO) Voltage Regulator that can operate with a very small Input–Output Differential Voltage with nm CMOS technology in turn increasing the Packing Density, provides for the new approaches towards power management is proposed. A Simple Symmetric Operational Trans-Conductance Amplifier is used as the Error Amplifier (EA), with a current splitting technique adopted to boost the gain. This also enhances the closed-loop bandwidth of the LDO Regulator. In the rail-to-rail output stage of the EA, a Power Noise Cancellation Mechanism is formed, minimizing the size of the Power MOS transistor. These advantages allow the proposed LDO Regulator to operate over a wide range of operating conditions while achieving maximum current efficiency, less output variation for a variable load transient, and effectively appreciable Power Supply Rejection Ratio. The compact area of the proposed LDO regulator leads to a chip area efficient low drop-out Voltage Regulator which finds its applications for portable electronics, i.e. cellular phones, pagers, laptops, etc.

Index Terms: 45nm CMOS Technology, Low Drop-Out Voltage Regulator, Low Power, Low quiescent current, PSRR.

I. INTRODUCTION

A low-dropout or LDO regulator is a DC linear voltage regulator which can operate with a very small input–output differential voltage[10]. The advantages of a low dropout voltage include a lower minimum operating voltage, higher efficiency operation and lower heat dissipation The increase in demand for portable appliances emphasize the necessity of complete system-on-chip (SOC) design solutions with smaller sizes and lower operating voltages[12]. The usage of the battery powered devices in today's global village has become pervasive and indispensable in almost every walk of life. The thrust is towards reducing the number of battery cells, required to decrease cost and size, while minimizing quiescent current flow to increase battery life. Current efficiency is particularly important because at low load current conditions and the life of the battery is adversely affected by low current efficiency or high current flow. In fact, the increasing drive towards total chip integration demands that power supply circuits be included in every chip. Low dropout regulators can be categorized as either low power or high power, low power LDO's are those with a maximum output current of less than 1A, exhibited by most portable applications. The operation of the LDO circuit is based on feeding back an amplified error signal to control the output current flow of the power transistor driving the load. In the design of LDO regulator, the main goal is to find the approach that allows one to avoid the on chip compensating capacitors, which occupy a large chip area and to achieve the required stability using external off-chip load capacitance only. Low dropout regulators are appropriate for many circuit applications namely, automotive, portable, industrial and medical applications. In the automotive industry, the low dropout voltage is necessary during cold-crank conditions where the battery voltage can drop below 6V. The voltage supplied out of the battery may vary instead of being a constant voltage for corresponding units. This gives rise to a situation where the entire system may get damaged.

The LDO array utilized in the power distribution system correspondingly distributes the regulated voltages to the units. Today's LDO's must meet demands of low operating voltages and low quiescent currents as a consequence of the higher packing densities that process technology demands. In this paper we are proposing LDO regulator which will be as compact as possible and because of this compact architecture it leads to a chip area efficient low drop- out voltage regulator which finds its applications for portable electronics, i.e., cellular phones, pagers, laptops, etc. The 45nm CMOS technology will provide new approaches towards power management in portable battery operated electronic devices.

From the rigorous review of related work and published literature, it is observed that many researchers have designed low drop - out regulator by applying different techniques. Researchers have undertaken different systems, processes or phenomena and focused on enhancing the transient response or the PSR or both of the LDO regulators. In the year 2005, 2008 P. Hazucha[9] , Y. H.[8] Lam respectively, in their papers stated that, "LDO regulators use either a large driving current or additional circuits, which consume a significant IQ". Recently in the year 2013, Chung-Hsun Huang[1], Member, IEEE, Ying-Ting Ma, and Wei-Chen Liao in their paper," Design of a Low-Voltage Low-Drop-Out Regulator", stated that, a low-voltage low-dropout (LDO) regulator converted an input of 1 V to an output of 0.85–0.5 V, with 90-nm CMOS technology. The current technology up to 2013 was higher range of nm technology. Hence considering the advancement of future technology the proposed project has been decided to do with the selection of lower order of nm technology.

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scope of work

The objective of this project is to enhance performance of low drop-out regulators for battery powered electronics. This is targeted to fulfill the present commercial requirements as well as the projected demands of the future. To design a low-dropout (LDO) voltage regulator that can operate with a very small input–output differential voltage with 45nm CMOS technology in turn increasing the packing density, provides for the new approaches towards power management is proposed.

II. LOW DROP-OUT REGULATOR

A. General Block Diagram

The supply voltage of a system-on-chip (SOC) is generally generated from an external supply voltage as shown in Fig. 1. First, the external supply voltage level is converted to another level with a switching DC-DC converter to get high power efficiency. Because the output voltage of a switching DC-DC converter can have large ripple, a low drop-out (LDO) regulator is followed to reject the ripple noise of the switching converter and finally the low drop out voltage is given to the desired load.

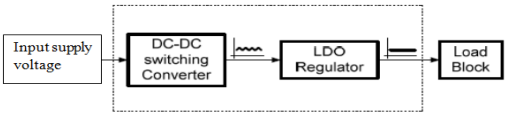

Fig. a: General block diagram of an LDO with a load

A simple symmetric operational trans-conductance amplifier is used as the error amplifier (EA), with a current splitting technique adopted to boost the gain. This also enhances the closed-loop bandwidth of the LDO regulator. In the rail-to-rail output stage of the EA, a power noise cancellation mechanism is formed, minimizing the size of the power MOS transistor. Furthermore, a fast responding transient accelerator is designed through the reuse of parts of the EA. Dropout voltage is the input-to-output differential voltage at which the circuit ceases to regulate against further reductions in input voltage; this point occurs when the input voltage approaches the output voltage and this is the basic function of a conventional LDO.

B. Conventional Block Diagram

Low-drop out regulators is one of the most conventional applications of operational amplifiers. Figure1 shows the basic topology. A voltage reference is used with the op-amp to generate a regulated voltage, Vreg. If the voltage reference is stable with temperature, the fact that the Vreg is a function of a ratio of resistors (so process or temperature changes in the resistance value don't affect the ratio) and the variation in the op-amp's open loop gain is desensitized using feedback makes the regulated voltage stable with process and temperature changes. The ideal (meaning that the op-amp has infinite open-loop gain) regulated voltage is [11]

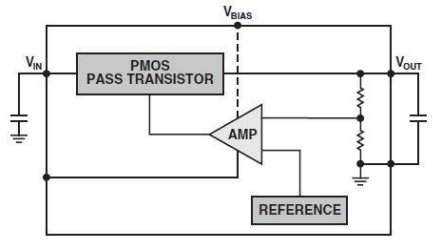

Fig. b: Conventional LDO

$V_{reg} = V_{ref}(1+R_1/R_2)$ (1)

If the op-ams's open loop gain is finite, then we can write

$V_{reg} = A_{o1}.(V_p-V_m)$ (2)

and

$V_m= V_{reg}(R_2/R_1+R_2)$ and $V_p= V_{ref}$ (3)

Solving for the actual regulated voltage, gives

$V_{reg} =V_{ref}(1/((1/A_{o1})+(R_2/(R_1+R_2))))$ (4)

III. SPECIFICATIONS OF LDO

1. REGULATION

Low-dropout (LDO) regulators work in the same way as all linear voltage regulators. The main difference between LDO and non-LDO regulators is their schematic topology. Instead of an emitter follower topology, low-dropout regulators utilize open collector or open drain topology. This enables transistor saturation, which allows the voltage drop from the unregulated voltage to the regulated voltage to be as low as the saturation voltage across the transistor.

If a bipolar transistor is used, as opposed to a field-effect transistor or JFET, significant additional power may be lost to control it, whereas non-LDO regulators take that power from voltage drop itself. For high voltages under very low In-Out difference there will be significant power loss in the control circuit.

Power FETs may be preferable to reduce power consumption, but this poses problems when the regulator is used for low input voltage, as FETs usually require 5 to 10V to close completely. Power FETs may also increase the cost. Our expected load & line regulation will be zero.

2. QUIESCENT CURRENT

Among other important characteristics of a linear regulator is the quiescent current, also known as ground current or supply current. Quiescent current is current drawn by the LDO in order to control its internal circuitry for proper operation. The series pass element, topologies, and ambient temperature are the primary contributors to quiescent current.

Many applications don't require an LDO to be in full operation all of the time (i.e. supplying current to the load). In this idle state the LDO still draws small amounts of quiescent current in order to keep the internal circuitry ready in case the load is enabled. When no current is being supplied to the load, P_{loss} can be found as follows:

$P_{loss} =V_{in} \times I_q$ (5)

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In order to minimize power loss while the LDO is idle, quiescent current should be as low as possible. Decreased power consumption allows portable applications to achieve longer battery life. It's also beneficial for enclosed applications that have trouble dissipating heat that may result from inefficient LDOs. To have a high efficiency, the quiescent current must be minimized.

3. POWER SUPPLY REJECTION

To provide a clean and accurate output voltage with a low voltage level (≤1 V), noise suppression is paramount. An n-type power MOS transistor or a cascaded power MOS transistor structure can achieve a high PSR; however, they are unfeasible for sub 1-V operations. As an LDO regulator adopts a p-type power MOS transistor, either a high loop gain or good noise cancellation can achieve a high PSR. It is, however, difficult to achieve a high loop gain with a low supply voltage. In addition, the circuit for the power noise cancellation mechanism increases the design complexity and consumes extra IQ.

Every step of design follows the design flow of MICROWIND 3.1 software. The design methodology will be according to VLSI backend design flow. The main target is to design and analyze the low drop-out regulator. To achieve the proposed target following steps are included in the design and analysis of low drop out voltage regulator.

IV. PROPOSED REGULATOR ARCHITECTURE

In the conventional architecture of the LDO, it is assumed that the error amplifier, by virtue of its large gain and resistive feedback, desensitizes variations in the gain so that a stable regulated voltage output is obtained. In our architecture, a current-sourcing PMOS in the output stage has been introduced. It is required that the PMOS be pulled all the way to ground so as to be biased further into saturation region. For this reason, the existing topology is modified and a common source stage is added; with the amplifying device being large enough so as to be a strong pull-down device. The common-source stage is responsible for enhancing signal swing and boosting.

The two gate inputs provided to the proposed LDO architecture will make the device programmable. Two bit binary values are given to the gate inputs. The variation of the output with respect to these inputs will be as depicted in the following table.

Binary input	Output voltage(V)
00	1.025
01	1
10	0.975
11	0.95

Table I: Variation in input and output

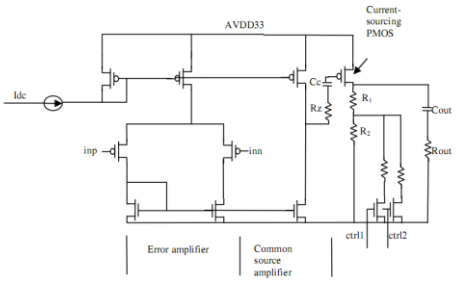

Fig. c: Schematic of proposed regulator

The proposed architecture consists of the following stages:

1. Error Amplifier
2. Common Source Amplifier
3. Current-sourcing PMOS

1. ERROR AMPLIFIER

A high gain operational amplifier is used as the error amplifier, with a stable voltage reference fed to one of its inputs. The voltage reference is usually derived from a band gap reference circuit. The differential pair of the operational amplifier consists of a current mirror NMOS load and a PMOS tail current source, with the gate-drain connected load being driven by a 2.5 uA ideal current source. A current mirror load has the advantage of providing high output impedance, and consequently, high gain. An operational amplifier connected with this sort of load is termed an open-transconductance amplifier, where all nodes are low impedance nodes with the exception of the differential pair.

2. COMMON-SOURCE AMPLIFIER

In general, a source follower is used as the buffer stage in most LDO's.The source follower has asymmetric current driving capability, and gain less than one. Hence a common-source amplifier is used, which has a small signal gain equal to

$$A_v=g_m(r_{o1}\| r_{o2}) \quad (6)$$

where gm is the transconductance of the amplifying device, ro1 and ro2 are the output resistances of the load and the amplifying device.

The equation implies that when the amplifying device (in our case, the NMOS) is made large enough, the gain at the second stage is improved. Proper sizing of the NMOS also ensures that it acts as a strong pull down, yielding rail-to-rail swing.

3. CURRENT-SOURCING PMOS

The sizing of the current-sourcing PMOS is the most vital part of the entire design. PFETs are known to have poor current driving capability, as a result of which a large-size PMOS is required. In our design, a PMOS with high voltage threshold (of up to 540 mV in slow corner) has been used. The question arises as to why a lower voltage threshold PMOS was not chosen, which might have provided the advantage of lesser area. Low-voltage threshold FETs are known to contribute to leakage currents, increasing power dissipation in the device. The PMOS is responsible for quick charging and discharging of

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the output node, thereby increasing slew rate to obtain faster settling times.

V. STEPS SPECIFYING DESIGN METHODOLOGY OF LDO

- Schematic design of proposed LDO using CMOS transistors.
- Performance verification of the above for different parameters.
- CMOS layout for the proposed LDO using VLSI backend.
- Verification of CMOS layout and parameter testing.
- If the goal is achieved for all proposed parameter including detail verification, sign off for the design analysis and design will be ready for IC making.
- If detail verification of parameters is not completed then again follow the first step with different methodology.

To achieve the low drop out regulator, different methodology and techniques can be used for research. The MICROWIND3.1 program allows designing and simulating an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. MICROWIND 3.1 includes all the commands for a mask editor as well as original tools never gathered before in a single module (2D and 3D process view, VERILOG compiler, tutorial on MOS devices). We can gain access to circuit simulation by pressing one single key. The electric extraction of circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

The current technology up to 2013 was higher range of nm technology. Hence considering the advancement of future technology and the advantage of 45nm technologies over 90 and 65nm technology, the proposed project has been decided to do with the selection of lower order of nm technology. Considering all these constraints regarding the demand of today's fast communication and mobile world, the research has been undertaken to design low power low drop-out chip area efficient voltage regulator using 45nm CMOS technology.

The proposed LDO is designed using 45 nm CMOS/VLSI technology in MICROWIND 3.1. The main novelties related to the 45 nm technology are high-k gate oxide, metal gate and very low-k interconnect dielectric. The effective gate length required for 45 nm technology is 25nm and these key features of 45 nm technologies are provided from various providers like TSMC, Fujitsu, Intel, etc. As compared to 65nm/90nm CMOS technology, 45 nm CMOS technology offers:

- 30% increases in switching performance
- 30 % reduction in Power consumption
- 2 times higher density
- 2 times reduction of the leakage between source and drain and through the gate oxide.

Considering the advantages of 45 nm technologies over 90 nm & 65 nm technologies, the proposed work of designing low drop-out voltage regulator is done with 45 nm CMOS technology.

VI. CONCLUSION

In conclusion, the paper has demonstrated the issues involved in designing a low drop-out regulator under existing process technologies meeting today's and tomorrow's market demands. The LDO design can be targeted for low load conditions and the input range can be widened with the help of design modifications. Different circuit topologies can further decrease dropout voltage of the LDO design. The proposed low-dropout regulator can operate with a very small input–output differential voltage, a minimum operating voltage, higher efficiency operation and lower heat dissipation.

REFERENCES

[1] Chung-Hsun Huang, Member, IEEE, Ying-Ting Ma, and Wei-Chen Liao," Design of a Low-Voltage Low-Dropout Regulator," May 2013

[2] Pappas, I. ; Kalenteridis , V. ; Siskos , S. ; Vlassis, "A complete over-current/short-circuit protection system for Low-Drop Out regulators," (2012)

[3] C. Chen, J. H. Wu, and Z. X. Wang, "150 mA LDO with self adjusting frequency compensation scheme," Electron. Lett., vol. 47, no. 13, pp. 767–768, Jun. 2011

[4] J. Hu, B. Hu, Y. Fan, and M. Ismail, "A 500 nA quiescent, 100 mA maximum load CMOS low-dropout regulator," in Proc. IEEE Int. ConfElectron. Circuits Syst., Dec. 2011, pp. 386–389.

[5] M. El-Nozahi, A. Amer, J. Torres, K. Entesari, and E. Sanchez-Sinencio, "High PSR low drop-out regulator with feed-forward ripple cancellation technique," IEEE J. Solid- State Circuits, vol. 45, no. 3, pp. 565–577,Mar. 2010.

[6] G. A. Rincon-Mora, Analog IC Design with Low-Dropout Regulators, New York, NY, USA: McGraw-Hill, 2009, Ch. 1.

[7] H.-C. Lin, H.-H. Wu, and T.-Y. Chang, "An active-frequency compensation scheme for CMOS low-dropout regulators with transient-response improvement," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 55, no. 9, pp. 853–857, Sep. 2008.

[8] Y.-H. Lam and W.-H. Ki, "A 0.9 V 0.35 μm adaptively biased CMOS LDO regulator with fast transient response," in Proc. IEEE Int. Solid-State Circuits Conf., Feb. 2008, pp. 442–443, 626.

[9] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan, and S. Borkar, "Area-efficient linear regulator with ultra-fast load regulation", IEEE J. Solid-State Circuits, vol. 40, no. 4, pp. 993–940, Apr. 2005.

[10] Gabriel A. Rincon-Mora, Member, IEEE, and Phillip E. Allen, Fellow, IEEE 1998 " A low-voltage, low quiescent current, low drop-out regulator"

[11] Naga Prasad Reddy, Martin, Chandra Mohan , Design and VLSI Implementation of Low Voltage and Low

[12] Dropout Voltage Regulator, International Journal of Computer Trends and Technology (IJCTT) – volume 4 Issue 8–August 2013.

[13] Books

[14] "Design of Analog CMOS Integrated Circuits", by Behzad Razavi.